Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently Amended) A Phase detector for a phase-locked loop for digital input signals in which the digital summed value for a particular number of bits is equivalent to zero, said phase detector having a plurality of sampled and digitized digital sample value [comprising a sampled and digitized data signal] being supplied to said phase detector, comprising a delay stage for delaying the digital sample values [data signal] by one or more sampling clock periods, a subtraction stage, to which the undelayed and the delayed digital sample values [data signal] are supplied to produce a differential value, and a filter or control stage, to which the output of the subtraction stage is supplied at the output of the filter or control stage which a [the] phase error can be tapped off, characterized in that a processing stage is provided, located between the subtraction stage and the filter or control stage, which assigns one of a [the] plurality of possible output values, to the [respective] differential value, wherein a full differential value range is subdivided in a number of sub-ranges corresponding to the [a] plurality of possible output values, so that each differential value falling within [all of the said differential values in] one of the sub-ranges will get a [the] same output value assigned.

2. (Currently Amended) The phase detector according to Claim 1, wherein the subtraction stage is integrated in a comparison stage which compares the delayed sample with said undelayed sample and assigns said one of a plurality of output values to the [respective] differential value.

3. (Previously Amended) The phase detector according to Claim 1, wherein said filter or control stage is a Proportional Integral (PI) controller.

4. (Previously Amended) The phase detector according to Claim 1, in which the delayed digital sample is deducted from the undelayed digital sample in the subtraction stage.

5. (Currently Amended) The phase detector according to Claim 1, in which a rectifier for signal conditioning is provided which has the sampled and digitized data signal supplied to it, the sampled and digitized data signal being a ternary data signal, in particular.

6. (Currently Amended) The phase detector according to Claim 5, in which the unrectified sampled and digitized ternary data signal is supplied[, before rectification,] to a separating stage in which the sampled and digitized data signal is separated into a positive and a negative path.

7. (Previously Amended) The phase detector according to Claim 6, in which separate delay, subtraction and processing stages or delay and comparison stages are provided for each path, and in which an addition stage is provided in which the assigned output values from one of either processing or comparison stages are added and, combined in this way, are passed on to the filter or control stage.

8. (Previously Amended) The phase detector according to Claim 7, in which, in addition to the separate delay, subtraction and processing stages or delay and comparison stages for the positive and the negative path, there are also separate delay, subtraction and processing stages or delay and comparison stages for a further path, in which the unrectified sampled and digitized ternary [complete] data signal is processed, the output values assigned by the processing stages or comparison stages of the further path likewise being supplied to the addition stage.

9. (Currently Amended) The phase detector according to Claim 1, wherein the phase detector is integrated in a phase-locked loop circuit for recovering the data clock signal for a sampled and digitized data [digital] signal.

10. (Currently Amended) The phase detector according to Claim 9, wherein the data signal delayed by one or more sampling clock periods corresponds to the data clock signal in the sampled and digitized data signal.